CLAIMS

WE CLAIM:

1. A method used in a spatial light modulator that comprises an array of pixels, wherein the pixels of each row of the array are divided into a plurality of subgroups, for producing an image, the method comprising:

receiving a set of pixel data streams, wherein the pixel data of each stream represent a set of states of a pixel of the spatial light modulator during different time intervals;

transforming the received pixel data streams into a set of bitplane data streams, wherein the bitplane data of each stream represent the states of a plurality of pixels during one time interval, such that the bitplane data streams representing the pixels of the same subgroup are parallel and adjacent; and

updating the states of the pixels using the transformed bitplane data.

2. The method of claim 1, wherein the bitplane data representing adjacent pixels of the spatial light modulator are parallel but not adjacent.

3. The method of claim 1, wherein the bitplane data streams representing the odd numbered pixels of the spatial light modulator are parallel and adjacent.

4. The method of claim 1, wherein the bitplane data streams representing the even numbered pixels of the spatial light modulator are parallel and adjacent.

5. The method of claim 1, wherein the state is selected from an ON state and an OFF state, and in the ON state, the pixel of the spatial light modulator represents a "bright" pixel of the image, and in the OFF state, the pixel represents a "dark" pixel of the image.

6. The method of claim 5, wherein the value of the pixel data determines the time duration of the pixel in the state.

7. The method of claim 1, wherein the time intervals are determined according to a pulse-width-modulation technique.

8. The method of claim 7, wherein the time intervals are determined according to a binary-weighted pulse-width-modulation technique.

9. The method of claim 1, further comprising:

storing the transformed bitplane data streams in a frame buffer having a plurality of storage regions such that the bitplane data streams representing the pixels of the same subgroup are stored consecutively in the same region of the frame buffer.

10. The method of claim 9, further comprising:

storing the transformed bitplane data streams in a frame buffer having a plurality of storage regions such that the bitplane data streams representing the pixels of separate subgroups are stored in different regions of the frame buffer.

11. The method of claim 9, further comprising:

upon receiving a writing signal,

retrieving the bitplane data of the first significance from a first region of the frame buffer; and

writing the pixels of the spatial light modulator with the retrieved bitplane data.

12. The method of claim 11, wherein the step of writing the pixels further comprises: activating the pixels using a first wordline.

13. The method of claim 12, further comprising:

retrieving the bitplane data of the second significance from a second region of the frame buffer; and

writing the pixels of the spatial light modulator with the retrieved bitplane data.

14. The method of claim 13, wherein the step of writing the pixels further comprises: activating the pixels using a second wordline.

15. The method of claim 13, wherein the pixel comprises a charge pump memory cell that further comprises:

a transistor having a source, a gate, and a drain;

a storage capacitor having a first plate and a second plate; and

wherein the source of said transistor is connected to a bitline, the gate of said transistor is connected to a wordline, and wherein the drain of the transistor is connected to the first plate of said storage capacitor forming a storage node, and wherein the second plate of said storage capacitor is connected to a pump signal.

16. A method used in a spatial light modulator that comprises an array of pixels, wherein the pixels of each row of the array are divided into a plurality of subgroups, for producing an image, the method comprising:

receiving a set of pixel data streams, wherein the pixel data of each stream represent a set of states of a pixel of the spatial light modulator during different time intervals;

transforming the received pixel data streams into a set of bitplane data streams according to a predetermined format, wherein the bitplane data of each stream represent the states of a plurality of pixels during one time interval, such that the bitplane data streams representing the pixels of different subgroups are interleaved; and

updating the states of the pixels using the transformed bitplane data.

17. The method of claim 16, wherein the state is selected from an ON state and an OFF state, and in the ON state, the pixel of the spatial light modulator represents a "bright" pixel of the image, and in the OFF state, the pixel represents a "dark" pixel of the image.

18. The method of claim 17, wherein the value of the pixel data determines the time duration of the pixel in the state.

19. The method of claim 16, wherein the time intervals are determined according to a pulse-width-modulation technique.

20. The method of claim 19, wherein the time intervals are determined according to a binary-weighted pulse-width-modulation technique.

21. The method of claim 16, further comprising:

storing the transformed bitplane data streams in a frame buffer having a plurality of storage regions such that the bitplane data streams representing the pixels of the same subgroup are stored consecutively in the same region of the frame buffer.

22. The method of claim 17, further comprising:

storing the transformed bitplane data streams in a frame buffer having a plurality of storage regions such that the bitplane data streams representing the pixels of separate subgroups are stored in different regions of the frame buffer.

23. The method of claim 21, further comprising:

upon receiving a writing signal,

retrieving the bitplane data of the first significance from a first region of the frame buffer; and

writing the pixels of the spatial light modulator with the retrieved bitplane data.

24. The method of claim 23, wherein the step of writing the pixels further comprises: activating the pixels using a first wordline.

25. The method of claim 24, further comprising:

retrieving the bitplane data of the second significance from a second region of the frame buffer; and

writing the pixels of the spatial light modulator with the retrieved bitplane data.

26. The method of claim 24, wherein the step of writing the pixels further comprises: activating the pixels using a second wordline.

27. A system comprising:

a memory cell array, wherein a row of said array comprises a first and second subset, each subset having one or more memory cells;

a first wordline and a second wordline, wherein the first wordline is connected to the first subset memory cells, and the second wordline is connected to the second subset memory cells;

a first set of data to be loaded into the first subset of memory cells that are activated through the first wordline, wherein the first set of data is consecutively stored in a first region of a storage medium; and

a second set of data to be loaded into the second subset of memory cells that are activated through the second wordline, wherein the second set of data is consecutively stored in a second region of the storage medium.

28. The system of claim 27, wherein the memory cell array is a portion of a spatial light modulator that comprises an array of pixel elements, each of which corresponds to a pixel of an image; and wherein each memory cell corresponds to at least one pixel element of the spatial light modulator.

29. The system of claim 28, wherein each pixel element of the spatial light modulator further comprises a movable mirror plate that is associated with a memory cell of the memory cell array, such that a state of the mirror plate is determined by the data stored in said memory cell.

30. The system of claim 28, wherein each memory cell is associated with a plurality of pixel elements of the spatial light modulator; and wherein the memory cell stores a data that determines a state of one of the plurality of pixel elements.

31. The system of claim 27, further comprising:

a plurality of bit lines connected to the storage medium and the memory cells such that the data stored in the storage medium are delivered into the memory cells via the bit lines.

32. The system of claim 27, wherein the first set of data and the second set of data are bit plane data.

33. The system of claim 27, wherein the first wordline connects the even numbered memory cells of the row, and the second wordline connects the odd numbered memory cells of the row.

34. The system of claim 27, wherein the first set of data is to be loaded into the even numbered memory cells of the row and the second set of data is to be loaded into the odd numbered memory cells of the row.

35. The system of claim 27, wherein the memory cells are charge-pump-memory cells, each of which further comprises:

a transistor having a source, a gate, and a drain;

a storage capacitor having a first plate and a second plate; and

wherein the source of said transistor is connected to a bitline, the gate of said transistor is connected to a wordline, and wherein the drain of the transistor is connected to the first plate of said storage capacitor forming a storage node, and wherein the second plate of said storage capacitor is connected to a pump signal.

36. The system of claim 27, wherein the memory cells are DRAM cells.

37. The system of claim 27, further comprising:

a data processing unit that is connected to the storage medium, and outputs bit plane data to the storage medium.

38. The system of claim 37, wherein the data processing unit further comprises:

a data converter that receives pixel data and outputs bit plane data.

39. The system of claim 38, wherein the converter is associated with a sequence of clock cycles.

40. The system of claim 39, wherein the converter further comprises:

a plurality of inputs, each input receiving a sequence of data signals;

a set of delay units connected to the input lines, each delay unit delaying a received data signal a predefined number of clock cycles; and

a switch connected to the delay units and the input lines for permuting received data between the input lines based on a predefined permutation rule.

41. The system of claim 40, wherein the delay unit comprises one or more flipflops.

42. The system of claim 40, wherein the delay unit is a shift-register.

43. The system of claim 40, wherein the switch comprises one or more multiplexers.

44. The system of claim 37, further comprising: an image source.

45. The system of claim 44, wherein the image source outputs an analog image signal.

46. The system of claim 44, wherein the image source is connected to the data processing unit such that the data processing unit receives the analog image signal and transforms the analog image signal into a bit plane data.

47. The system of claim 44, wherein the image source outputs pixel image data complying with a pixel data format.

48. A method for writing a memory cell array, wherein a row of the memory cell array comprises a first and second subset of memory cells, each subset having one or more memory cells, the method comprising:

connecting the memory cells of the first subset to a first wordline, and the memory cells of the second subset to a second wordline;

storing a first and second set of data such that the data of the first set are stored consecutively in a first region and the data of the second set are consecutively stored in a second region separate from the first region;

activating the memory cells of the first subset through the first wordline; and

loading the first set of data into the activated first subset of memory cells.

49. The method of claim 48, further comprising:

activating the memory cells of the second subset through the second wordline; and

loading the second set of data into the activated second subset of memory cells.

50. The method of claim 48, wherein the step of storing the first and second set of data further comprises:

storing a first set of bit plane data in the first region, and a second set of bit plane data other than the first set of bit plane data in the second region.

51. The method of claim 48, further comprising:

connecting each memory cell to an electrode such that an electrical potential of the electrode is determined by the data stored in said memory cell.

52. The method of claim 51, further comprising:

disposing the electrode proximate to a mirror plate of a micromirror such that an electrostatic field is established between the electrode and the mirror plate, and the mirror plate rotates in response to the established electrostatic field.

53. The method of claim 48, further comprising:

receiving a sequence of analog signals representing an image;

transforming the analog signals into a set of bit plane data complying with the bit plane format.

54. The method of claim 53, further comprising:

transforming the analog signals into a set of pixel data complying with the pixel data format; and

converting the set of pixel data into the set of bit plane data.

55. The method of claim 54, wherein the step of converting the set of pixel data into the set of bit plane data further comprises:

loading the pixel data as a pixel data matrix; and

transposing the pixel data matrix.

56. The method of claim 55, wherein the step of transposing the pixel data matrix further comprises:

delivering the pixel data into a plurality of input lines that are associated with the sequence of clock cycles;

delaying the pixel data with reference to the sequence of clock cycles according to a predefined delay scheme; and

permuting the pixel data between the input lines based on a predefined permutation scheme.

57. The method of claim 56, wherein the step of delaying is performed by one or more standard flipflop circuits.

58. The method of claim 56, wherein the step of delaying is performed by a shift-register.

59. The method of claim 56, wherein the step of switching is performed in response to one or more switch signals.

60. The method of claim 59, wherein the switch is performed by a multiplexer having an input for the switch signal.

61. The method of claim 48, further comprising:

providing the memory cell array as a portion of a spatial light modulator that comprises an array of pixel elements, each of which corresponds to a pixel of an image; and wherein each memory cell corresponds to at least one pixel element of the spatial light modulator.

62. The method of claim 61, wherein each pixel element of the spatial light modulator further comprises a movable mirror plate that is associated with a memory cell of the memory cell array, such that a state of the mirror plate is determined by the data stored in said memory cell.

63. The system of claim 61, wherein each memory cell is associated with a plurality of pixel elements of the spatial light modulator; and wherein the memory cell stores a data that determines a state of one of the plurality of pixel elements.

64. A system comprising:

a data converter having a plurality of inputs and outputs, wherein the data converter transposes a first data matrix into a second data matrix;

a first storage medium that is connected to the outputs of the data converter and consecutively stores a first portion of the second data matrix;

a second storage medium that is connected to the outputs of the data converter and consecutively stores a second portion of the second data matrix; and

wherein the first portion and the second portion are interleaved in the second data matrix.

65. The system of claim 64, wherein the first storage medium and the second storage medium are two regions of a frame buffer.

66. The system of claim 64, further comprising:

an array of memory cells, wherein a row of the array comprises a first and second subset, each subset having one or more memory cells; and

a first wordline and second wordline, wherein the first wordline is connected to the first subset memory cells and the second wordline is connected to the second subset memory cells.

67. The system of claim 66, wherein each memory cells is associated with a mirror plate of a micromirror that corresponds to a pixel of an image.

68. The system of claim 66, wherein the memory cell array is a portion of a spatial light modulator that comprises an array of pixel elements, each of which corresponds to a pixel of an image; and wherein each memory cell corresponds to at least one pixel element of the spatial light modulator.

69. The system of claim 66, wherein each pixel element of the spatial light modulator further comprises a movable mirror plate that is associated with a memory cell of the memory cell array, such that a state of the mirror plate is determined by the data stored in said memory cell.

70. The system of claim 66, wherein each memory cell is associated with a plurality of pixel elements of the spatial light modulator; and wherein the memory cell stores a data that determines a state of one of the plurality of pixel elements.

71. The system of claim 66, wherein the array of memory cells further comprises: a plurality of bit lines that are connected to the memory cells and the frame buffer such that the data are delivered into the memory cells via the bit lines.

72. The system of claim 64, wherein the data stored in the first storage medium are loaded into the memory cells that are activated by the first wordline.

73. The system of claim 72, wherein memory cells loaded with the data stored in the first storage medium are even numbered memory cells of the row of the memory cell array.

74. The system of claim 72, wherein the data stored in the second storage medium are loaded into the memory cells that are activated by the second wordline.

75. The system of claim 74, wherein memory cells loaded with the data stored in the second storage medium are odd numbered memory cells of the row of the memory cell array.

76. The system of claim 64, wherein the memory cell is a "charge-pump-memory cell", that further comprises:

a transistor having a source, a gate, and a drain;

a storage capacitor having a first plate and a second plate; and

wherein the source of said transistor is connected to a bitline, the gate of said transistor is connected to a wordline, and wherein the drain of the transistor is connected to the first plate of said storage capacitor forming a storage node, and wherein the second plate of said storage capacitor is connected to a pump signal.

77. The system of claim 64, wherein the memory cell is a DRAM cell.

78. The system of claim 64, further comprising:

a data processing unit that is connected to the storage medium, and outputs bit plane data to the storage medium.

79. The system of claim 78, wherein the data processing unit further comprises:

a data converter that receives pixel data and outputs bit plane data.

80. The system of claim 79, wherein the data converter is associated with a sequence of clock cycles.

81. The system of claim 64, wherein the first data is a pixel data.

82. The system of claim 64, wherein the second data matrix is a bit plane data matrix.

83. The system of claim 79, wherein the data converter further comprises:
a plurality of input lines for receiving a set of data of the first data matrix;
a set of delay units connected to the input lines for delaying the data with reference to a sequence of clock cycles according to a predefined delay scheme;
one or more switches connected to the input lines and delay units for permuting data between input lines based on a predefined permutation scheme; and
a plurality of outputs for outputting the data of the second data matrix;

84. The system of claim 83, wherein the delay unity is a flipflop.

85. The system of claim 83, wherein the delay unit is a shift-register.

86. The system of claim 83, wherein the switch comprises a multiplexer.

87. The system of claim 64, further comprises: an image source.

88. The system of claim 87, wherein the image source outputs a sequence of analog signals representing an image.

89. The system of claim 88, wherein the sequence of analog signals are transformed by the processing unit into a set of pixel data.

90. The system of claim 88, wherein the image source outputs a set of pixel data complying with the pixel data format.

91. A system, comprising:

a data processing unit that receives a first set of data and outputs a second set of data other than the first set of data;

a first storage medium that is connected to the outputs of the data processing unit and consecutively stores a first portion of the second set of data;

a second storage medium that is connected to the outputs of the data converter and consecutively stores a second portion of the second set of data;

an array of memory cells, wherein a row of the array comprises a first and second subset, each subset having one or more memory cells;

a first wordline and second wordline, wherein the first wordline is connected to the first subset memory cells and the second wordline is connected to the second subset memory cells; and

wherein the data stored in the first storage medium is to be loaded into the memory cells connected to the first wordline, and the data stored in the first storage medium is to be loaded into the memory cells connected to the first wordline.

92. The system of claim 91, wherein each memory cells is associated with a mirror plate of a micromirror that corresponds to a pixel of an image.

93. The system of claim 91, wherein the first set of data complies with the pixel data format and the second set of data complies with the bit plane data format.

94. The system of claim 91, wherein the array of memory cells further comprises: a plurality of bit lines that are connected to the memory cells and the frame buffer such that the data are delivered into the memory cells via the bit lines.

95. The system of claim 93, wherein the memory cell is a charge-pump-memory cell that further comprises:

a transistor having a source, a gate, and a drain;

a storage capacitor having a first plate and a second plate; and

wherein the source of said transistor is connected to a bitline, the gate of said transistor is connected to a wordline, and wherein the drain of the transistor is connected to the first plate of said storage capacitor forming a storage node, and wherein the second plate of said storage capacitor is connected to a pump signal.

96. A computer-readable medium having computer executable instructions for performing a method of writing a memory cell array, wherein a row of the memory cell array comprises a first and second subset of memory cells, each subset having one or more memory cells, and wherein the memory cells of the first subset are connected to a first wordline, and the memory cells of the second subset are connected to a second wordline, the method comprising:

storing a first and second set of data such that the data of the first set are stored consecutively in a first region and the data of the second set are consecutively stored in a second region separate from the first region;

activating the memory cells of the first subset through the first wordline; and

loading the first set of data into the activated first subset of memory cells.